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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,424	02/15/2001	Youri Ponomarev	NL 000139	7700

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER

ESTRADA, MICHELLE

ART UNIT	PAPER NUMBER
	2823

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/784,424	PONOMAREV, YOURI
	Examiner Michelle Estrada	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 19 June 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892) 2) <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s) _____ . 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____ .
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DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hwang et al. (EU-0614226), Aitken et al. (5,268,324) and further in view of Song (5,760,420).

Hwang et al. discloses a semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate (3) and which adjoin a surface thereof, which surface is provided with a layer of gate oxide (2) on which gate electrodes are formed at those areas of the semiconductor zones which form gate zones of these transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$; $0 < x < 1$) situated between said polycrystalline silicon layer and the gate oxide, (Col. 1, lines 43-50 and Col. 3, lines 15-20); having PMOS transistors having gate electrodes which are formed in a layer of p-type doped polycrystalline silicon without germanium situated in the gate oxide, the latter PMOS transistors being equal to the former in all other aspects (Col. 3, lines 25-40).

Hwang et al. does not disclose an amorphous silicon formed between the gate oxide layer and the layer of polycrystalline silicon; and characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium.

Aitken et al. disclose a CMOS structure characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium (Col. 1, lines 18-30 and fig. 1D).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hwang et al. and Aitken et al. to enable formation of the CMOS structure, and further it will increase the switching speed of the PMOS toward the level of that of the NMOS, it will increase the hole mobility of the PMOS.

Song discloses a substrate (11); a gate insulator (31); an amorphous silicon layer (41) and a silicon germanium layer (51); wherein the amorphous silicon layer is formed between the gate insulator and the silicon germanium layer (See fig. 3B).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hwang et al., Aitken et al. and Song to enable formation of the silicon germanium layer and further provides resistance to the structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is (703) 308-0729. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



George Fourson
Primary Examiner
Art Unit 2823



MEstrada
August 4, 2003